ABSTRACT

The invention has been made to provide a method of adjusting the clock delay by carrying out timing control including the synchronization of a clock delay in each hierarchical block and timing control in consideration of the synchronization of a clock delay over a hierarchical top.

A clock delay adjusting method of a semiconductor integrated circuit device, wherein a plurality of source points for adjusting a clock delay is provided to synchronize a value of the clock delay from each of the source points of each of hierarchical blocks in a semiconductor chip to a clock input circuit to be operated synchronously with a clock depending on a circuit design condition of the hierarchical block, and an area terminal is provided in the source point, and a clock input terminal of the semiconductor chip and each area terminal are connected through a clock line so as to be clock distributed over a hierarchical top and a clock delay between the hierarchical blocks is adjusted.